The Enhanced Performance of the DCC Current Comparator using AccuBridge® Technology

Duane Brown[1], Andrew Wachowicz[2], Shiping Huang[3]

[1]Measurements International, Prescott Canada duanebrown@mintl.com, [2]Andrew Wachowicz mieng1@mintl.com, [3]Shiping Huang mieng4@mintl.com

***Abstract* — The Direct Current Comparator (DCC) resistance bridges have been used to measure the Quantum Hall value with errors of 0.02 ppm or less (k=2). By improving the technologies described in the paper, the reduction of the inherent ratio error and stability due to the partial turns resolution and the linearity error of the nanovolt amplifier can reduce the bridge error to less than 0.01 ppm when used to measure the I = 2 plateau. Automatic balancing facilitates a Nano measurement operation of the bridge for more accurate resistance measurements of the QHR value.**

Key Words: Direct Current Comparator (DCC), AccuBridge®, ratio error, improved partial turn technology, ampere turns, variable slave turns, turns calibration, voltage balancing, and PID controller.

I. Introduction

The conventional DCC Ratio Bridge error ranges from 0.02 ppm to 0.01 ppm accuracy level for ratios of 1:1 to 10:1, while the AccuBridge® technology (Figure 1) has achieved the accuracy to be better than 0.01 ppm in the range of 13 kohm and less, and less than 0.05 ppm in the 100 kohm range. Although the present AccuBridge® technology has performed well by using the several achievements described in [3], there are some uncertainties and behaviours that need to be improved on by

- Reducing the deviation and error of the DCC turns (which consist of both the Master and Slave turns), to increase the accuracy and decrease the noise.
- Eliminating the residual flux in the DCC during operation which results in interchange errors and uncertainties.
- Eliminating the effects of the DCC hysteresis, caused by the levels of the ramping overshoot when the loads vary, and the proper timing when both the master and slave currents reverse.
- Improving the sensitivity and stability of the nanovolt detector to improve the noise to signal ratio and reduce the linearity error of the amplifier.

II. Present Status of 6010D Bridge

Several Bridges have been verified against the CCC at both NRCC and METAS (Table 1). Errors between the two have been less than 0.01 ppm with combined uncertainties of <0.02 ppm.

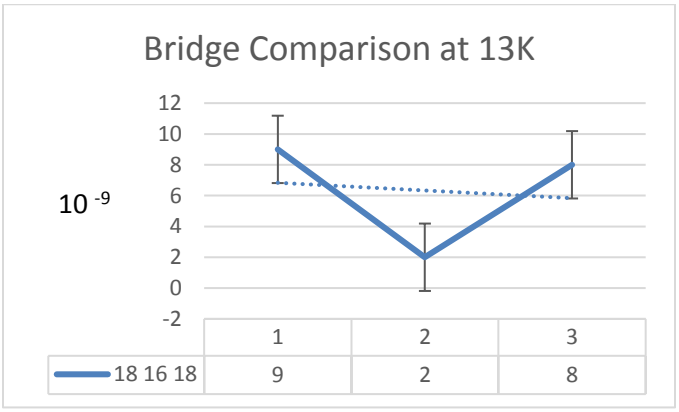

Chart 1: Three 6010Q Bridges Results & Uncertainties at 12906.4035Ω:1000Ω

III. A DCC Bridge Stability

Bridge Stability is determined by having a bridge verified over a three year time span.

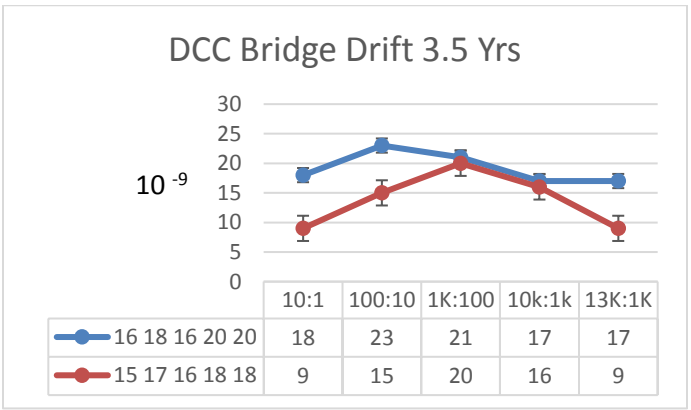

Chart 2: DCC Bridge Drift 3.5 years (10^{-9})

The conventional DCC Bridge Block Diagram is shown in Figure 1 with the ratio of Nx/Ns =Is/ Ix=Rx/Rs.

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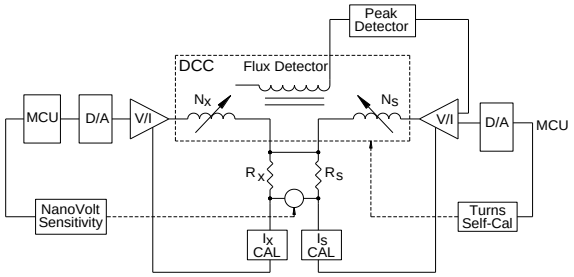


Fig.1. DCC Block Diagram

IV. TECHNOLOGY STRATEGIES

As known, the most errors in the interchanges and standard deviations, are reflected in the residual flux or hysteresis of the DCC magnetic field. In the current bridges or technology, that residual flux is eliminated by the balancing procedure of the turns with 1/128 resolution, the residue being corrected by the peak detector feedback. Due to the remaining flux, the actual numbers of the DCC turns, master or slave or both, are adjusted to the correct values for balancing the flux to 0. The errors and deviations associated to the peak detector and nanovolt amplifier are represented at the Nano-detector's input signal (V_n) for the signal processing in the firmware.

The error signals of the DCC are varied with and depend on the loads and currents. The Nano-detector sensitivity (gain) needs to be adjusted with the changes of the load but it is not easy to manage or optimize the proper gain for the best performance in all ranges. The accuracy and stability can also be affected by the gain.

In the dcCCC two new approaches in correcting the DCC Errors are considered as follows:

1. Increasing the resolution of both the Master (Nx) and Slave turns (Ns) which will reduce the window size that the nanovolt has to interpret.

2. A new approach using a voltage feedback with a ampere-turn balance, called Voltage Feedback Balance (VFB), is represented as a solution to make the V_n as small and stable as possible, and to take the advance for achieving the Nano-detector management which includes nanovolt calibration at the time of measurement The block diagram is shown in Figure 2 and the principle is illustrated below.

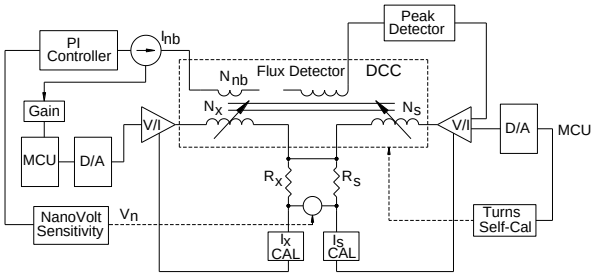


Fig.2. Enhanced AccuBridge® Block Diagram

In the voltage feedback balance (VFB) method, one extra winding (N_{nb}) is added in the ADCCC core to form a 4 windings group along with the master (N_x), slave (N_s) and Flux Detector windings. The nano-detector signal (error signal, V_n) acts as the feedback input to eject a current I_{nb} through N_{nb} by the conditional stage and a PI controller. When the dcCCC is at balance, the following equations should meet as V_n=0, by

$$-R_x I_x + R_s I_s = 0 \quad (1)$$

being for the voltage loop, and

$$N_x I_x - N_s I_s + N_{nb} I_{nb} = 0 \quad (2)$$

being for the resulting flux in the dcCCC core, with the peak-detector assumed at balance. The following equation is derived from Equation 1 and Equation 2,

$$\frac{Rx}{Rs} = \frac{Nx}{Ns}\left(1+ \frac{N_{nb} I_{nb}}{N_x I_x}\right) = \frac{N_x + {N_{nb} I_{nb}}/{I_x}}{N_s} = \frac{N_x + \Delta N_x}{N_s} \quad (3)$$

ΔN_x is the master deviation turns given by

$$\Delta N_x = N_{nb} \frac{I_{nb}}{I_x} \quad (4)$$

ΔN_x is an equivalent deviation turns with the master turn as the compensation for the ratio, and is manipulated in the micro-processing code.

V. SYSTEM DESIGN AND CONFIGURATIONS

The VFB architecture is composed of the analog-front, variable sensitivity, a proportional–integral (PI) controller, VFB current detector and the switching module for the operational sequences.

The prototype for the VFB unit has been designed and implemented to realize the functionalities described in the previous section in test and verification.

- This is a real time loop for controlling the V_n behaviors at balance.
- As the demand of lower noise and deviation for the Nano-detector error signal V_n, an analog-front amplifier is required with the ultra-low drift, noise and dc-offset. Hence using the existing operational amplifier module in AccuBridge® is for the error detecting.
- A proportional–integral (PI) controller is designed with the variable gain and integrated time for controlling the accuracy of the current (I_{nb}) and improving the stability.
- Adopting a derivative (D) controller as an option to speed up the control procedure but not sure how the stability is affected.
- A proposal resistor (100 kohm) to sense the VFB current I_{nb} that is measured in the digital processing for the ratio compensation.
- The VFB is functioned (switched) in the measurement system, after a few normal measurements (2 to 5) in order

to make less timing and more stable during the PI control procedure and less overshoot appears in the DCC.

- In order to minimize the ratio errors in the early stage of the measurement for V_n, the partial turn (PT) resolution was increased, which can be realized by increasing the number of the PT, shown in Figure 3. PT1 and PT2 have a resolution of 1/128 turns, and combined PT1 and PT2 give a resolution of 1/16384. It has the advantage in the pre-operation for the Nan-detector to adjust the allowed ratio within a much smaller margin (window).

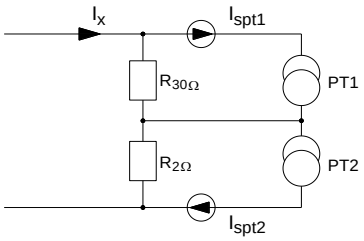
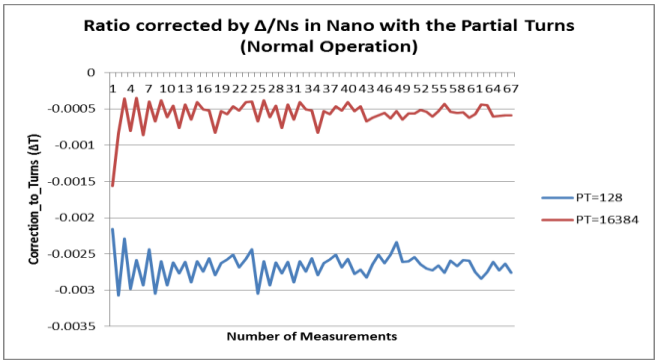


Fig.3. Partial Turn in high resolution

In the graph below illustrates the effects of the 1/16384 partial turns (PT) resolution is compared to PT of 1/128 partial turns. The equivalent turn's error is decreased from 0.0027 (blue curve) to 0.0005 (red curve), which is processed by the Nano-detector for the ratio corrections and down to

1) 0.24ppm from 1.3ppm for 1:1 or 1:10 ratio measurement (Ns=2048)
2) 0.98ppm from 5.3ppm for 10:1 ration measurement



(Ns=512)

Fig.4 Effects of the PT in the normal operation

VI. THE VFB PROTOTYPE AND EXPERIMENTS

The implemental system of the Enhanced AccuBridge as Figure 2, with a VFB prototype has been built in for verifying the functionality and performance in Figure 5. The achievable and major considerations on

- A proper number of the winding (N_{nb}) on the comparator to be selected for all ranges
- A sensitive amplifier with the variable gain to be set as the analog interface in the front of VFB in the certain range measurement
- PID controlling parameters optimized
- The current through the N_{nb} is detected in precision
- Accuracy and stability
- Noise and dc-offset at.

Fig.5 the Present System with the VFB Prototype

In the graph below the effects of the 1/16384 PT turns are compared to the PT of 1/16384 partial turns in VBF operation. The turn's error between both PTs is almost same as in normal operation and response represents the slight stronger in the fluctuation with a PID controlling feedback.

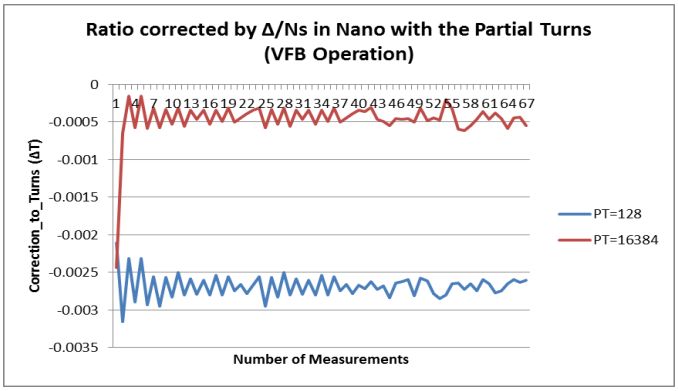


Fig.6 Effects of the PT in the VFB operation

In the enhanced system, the turn's error or ΔT is derived from Equation 4, and information needed to know the overall nano sensitivity (gain) rather than the fixed gain determined in the normal operation. The VFB method is a simple way to determine the turn's error by detecting the current (Inb) through the VFB winding (N_{nb}). The ratio errors are represented for the ratio correction, related with the accuracy and drift of the I_{nb}, I_x and N_{nb}.

The following results show that the performance with the VFB prototype, on the charicteristics in the stability, accuracy and noise level.

1. The repeatable (dispersible) for the ratio is affected with the VFB stable peformance, the resistor's drift, uncertainty of the unit and the environment status. The results in Fig.7 to Fig.8 show the ratio in 10:1ratio.
2. The standard deviation and interchange error give the part of the perspect for the performance in the noise-level and

accuracy. The results in Fig.9 to Fig.11 show the ratio in 1:1ratio, compared in the both Normal and VFB operation.

3. The Table1 summary the average values as the above results.

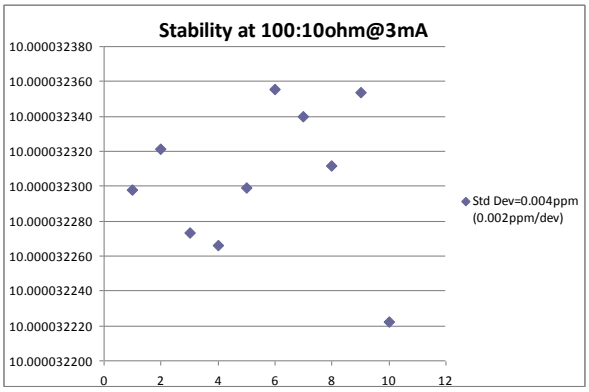


Fig.7 Ratio repeatable test with 100Ω:10Ω at 3mA

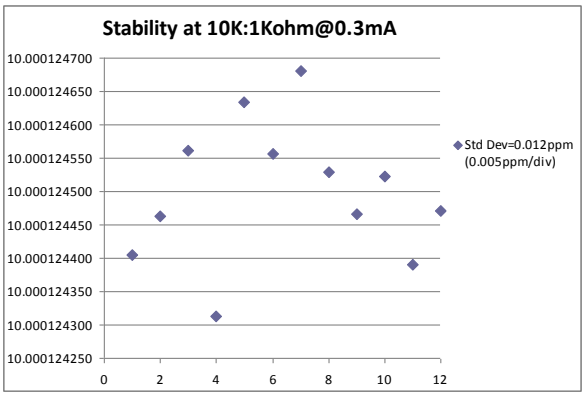


Fig.8 Ratio repeatable test with 10kΩ:1kΩ at 3mA

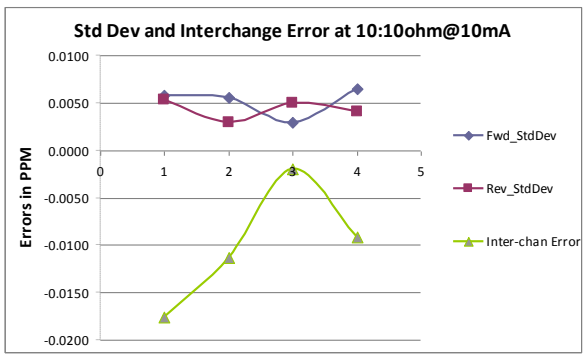


Fig.9 Standard Deviation & Interchange Error Test with 10Ω:10Ω at 10mA

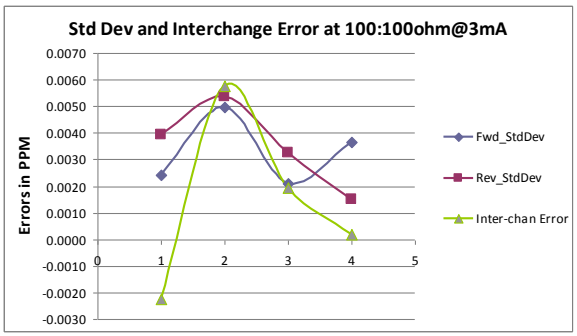


Fig.10 Standar Deviation & Interchange Error Test with 100Ω:100Ω at 10mA

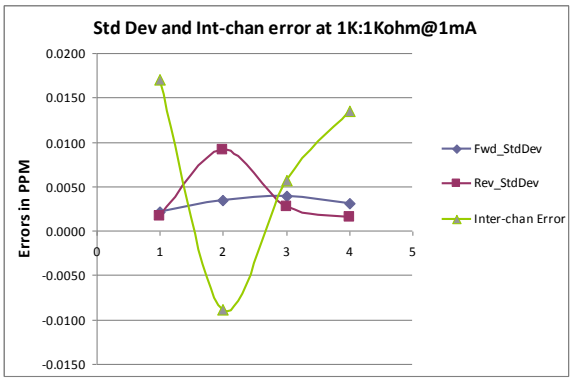


Fig.9 Standard Deviation & Interchange Error Test with 1kΩ:1kΩ at 0.3mA

VII. CONCLUSION

The results using the VFB prototype shows that the standard deviations in most ranges is now < 0.01 ppm, and the interchange errors are < 0.02 ppm. Some ranges showed a significant drop in the standard deviation and more stable status of the measurement. The uncertainty contributors associated to the VFB sensitivity, ampere-turn, dc-offset, modulation and power line AC signal (noises) are reduced to <0.005 ppm.

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